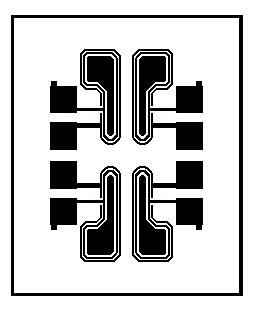
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.035”**

**.043”**



**D**

**D**

**D**

**D**

**S**

**S**

**S**

**G**

**S**

**G**

**G**

**G**

**SD5000**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .004” X .004”**

**Backside Potential: -**

**Mask Ref: CD2**

**APPROVED BY: DK DIE SIZE .035” X .043” DATE: 8/25/21**

**MFG: CALOGIC THICKNESS .009” P/N: SD5501**

**DG 10.1.2**

#### Rev B, 7/19/02